What is claimed is:

1. A method of controlling an integrated circuit (IC) to which inputs and outputs (I/Os) are separately provided and to which a write address and a read address are simultaneously input during one period of a clock signal, the method comprising:

(a) receiving a write address, a read address, and write data;

(b) determining, a memory block and a data memory block in which a data read operation and a data write operation are to be performed in response to the write address and the read address;

(c) performing the data read operation or the data write operation in the data memory block according to the determination of step (b); and

(d) performing the data read operation or the data write operation in the memory block according to the determination of step (b).

2. The method of claim 1, wherein step (b) is performed by a tag memory controlling unit.

3. The method of claim 1, wherein step (d) further comprises:

(d1) when the data read operation is performed, transmitting the read data to a transmitting unit corresponding to a sub-memory block inside the memory block;

(d2) transmitting the data transmitted to an output buffer; and

(d3) outputting the data transmitted to the output buffer.

4. The method of claim 3, wherein steps (a) through (d) each represent a stage of a pipeline in a pipeline structure in which an operation of the IC is performed.

5. The method of claim 4, wherein at least one stage operates during one period of a clock signal or during several periods of the clock signal.

6. The method of claim 5, wherein step (c) further comprises:

writing information regarding the data read or write operation performed in the data memory block to the tag memory controlling unit.

7. The method of claim 6, wherein in step (b), the information and an address of a tag memory in which the information is to be written are temporarily stored in a register before the information is written to the tag memory controlling unit.

8. The method of claim 7, wherein in step (b), when a newly received write or read address is coincident with the address of the tag memory in which the information is to be written, a subsequent operation is performed using the information stored in the register.

9. The method of claim 4, wherein as a result of step (b), when the operation of step (c) is not performed, the operation of step (d) is not performed at a stage corresponding to step (c), and no operation is performed at the stage corresponding to step (c).

10. The method of claim 1, wherein if the upper addresses of the received write address and read address are the same, the read address and the write address are not the same as a data memory address and data stored in the data memory block corresponding to the write address is valid, step (c) further comprises:

(c1) reading data stored in the data memory block corresponding to the write address; and

(c2) writing write data corresponding to the write address to the data memory block from which the data is read; and

step (d) further comprises:

(da) performing a data read operation in a sub-memory block corresponding to the read address; and

(db) writing the read data to a sub-memory block in which data read in step (c1) is stored.

11. The method of claim 10, wherein step (c2) further comprises (c21) writing the information regarding the write data written to the data memory block from which the data is read to the tag memory controlling unit.

12. The method of claim 10, wherein the data memory address is an address of the sub-memory block corresponding to the data memory block.

13. The method of claim 1, wherein the IC comprises a plurality of the memory blocks, each of the memory blocks comprising a plurality of sub-memory blocks, the data memory blocks corresponding to the memory blocks, and a tag memory controlling unit.

14. The method of claim 13, wherein the tag memory controlling unit writes data to the memory blocks or reads data from the memory blocks in response to the write address or the read address.

15. A method for performing a write operation and a read operation in an integrated circuit (IC) comprising a separate input and output (I/O), the method comprising:

receiving a write address, a read address and a write data command during a period of a clock signal;

determining, a first memory location and a second memory location, where a write operation and a read operation are to be performed in response to the write address and the read address; and

performing the write operation in one of the first memory location and the second memory location and the read operation in one of the first memory location

and the second memory location.

16. The method of claim 15, wherein the first memory location is a memory block and the second memory location is a data memory block.

17. The method of claim 15, wherein the determination step is performed by a memory controlling unit.

18. The method of claim 15, wherein the determination step further comprises:

determining if the write address and the read address are input;

determining if an upper address of the write address is coincident with an upper address of the read address;

determining if the write address and the read address are coincident with a data memory address; and

determining if data stored in one of the first memory location and the second memory location is valid data.

19. The method of claim 18, wherein the performing step further comprises:

performing the write operation or the read operation in one of the first memory location and the second memory location, when the operation to be performed corresponds to the address coincident with the data memory address;

performing the read operation in one of the first memory location and second memory location, when the write address and the read address are coincident with the data memory address;

storing new data in one of the first memory location and the second memory location, when data stored in one of the first memory location and the second memory location is valid data; and

writing the new data to one of the first memory location and the second memory location, when data stored in one of the first memory location and the second memory location is not valid data.

20. The method of claim 18, wherein the performing step further comprises:

performing the write operation or the read operation in a third memory location, when the operation to be performed corresponds to the address not coincident with the data memory address;

performing the write operation in the third memory location, when the write address and the read address are coincident with the data memory address;

storing new data in one of the first memory location and the second memory location, when data stored in one of the first memory location and the second memory location is valid data; and

writing the new data to one of the first memory location and the second memory location, when data stored in one of the first memory location and the second memory location is not valid data.

21. The method of claim 20, wherein the third memory location is a sub-memory block.